**Digital Systems Design Lab Exam Spring 2022**

**Write a Verilog code to implement a car parking system using FPGA.**

In the entrance of the parking system, there is a sensor which is activated to detect a vehicle coming. Once the sensor is triggered, a bulb turns on and a password is requested to open the gate. Take the binary representation of the last two digits of your registration number as password for the gate. If the entered password is correct, the gate would open to let the vehicle get in. Otherwise, the gate is still locked. Once the car enters the parking, the bulb is turned off. In case of wrong password if the car leaves the bulb turns off.

Use state machines (mealy/moore) to implement the above functionality. Draw the state diagram on the answer sheet provided to you.

**Outputs:**

Bulb (Turns on when vehicle is detected)

Gate (Turns on when the correct password is entered)

State (Display the states on 7 segment display)

Exam Marking Rubrics:

|  |  |  |
| --- | --- | --- |
|  | Total Marks | Obtained Marks |
| Output on FPGA | 5 points |  |
| Code synthesis without errors | 3 points |  |
| Clock divider | 4 points |  |
| Level to pulse converter | 4 points |  |
| Seven segment decoder | 4 points |  |
| State transition diagram | 5 points |  |
| Car parking system | 9 points |  |